ISSN:0975-9646

A Low Power and High Speed Design for VLSI Logic Circuits Using Multi-Threshold Voltage CMOS Technology

Phani kumar M, N. Shanmukha Rao

Dept. of ECE, MVGR College of Engineering, Andhra Pradesh, India

***Abstract*— In CMOS logic circuits, the reduction in the threshold voltage due to voltage scaling leads to increase in the subthreshold leakage current and hence static power dissipation. Although power consumption is important for modern VLSI design, operation speed and occupied area are still the main requirements of the VLSI design. Multi threshold voltage CMOS (MTCMOS) technology is a good solution which provides a high performance and low-power design without any area overhead. MTCMOS technology provides the transistors that have low, normal and high threshold voltage. The low-threshold voltage transistors are used to reduce the propagation delay time in the critical path, the high-threshold voltage transistors are used to reduce the power consumption in the shortest path. This paper describes a low-power and high speed design for full adder, 4-bit ripple carry adder and 4×4 multiplier circuits with MTCMOS technology using 45nm technology.**

***Keywords*— Multi-threshold voltage CMOS (MTCMOS), static power consumption, propagation delay.**

I. INTRODUCTION

Power dissipation is an important consideration in the design of CMOS logic circuits. In the present deep-submicron era, supply voltages and threshold voltages for MOS transistors are greatly reduced. This to an extent reduces the dynamic (switching) power dissipation. However, the subthreshold leakage current increases exponentially thereby increasing static power dissipation. Leakage current is the current that flows through a transistor when it is switched off. It depends on gate length, oxide thickness and varies exponentially with threshold voltage, temperature and other parameters.

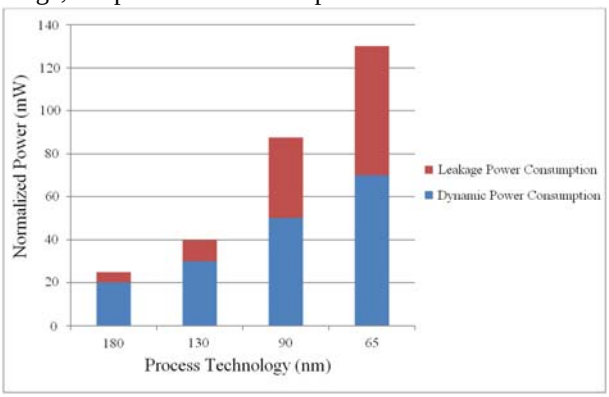


Fig. 1 Leakage and dynamic power consumption with technology scaling.

Scaling down of threshold voltage V_t results in exponential increase of the subthreshold leakage current [2], [3]. It can be seen from Fig.1 that the leakage power is very less compared to the dynamic power for 180nm technology. When the technology scaling reached 65nm, the leakage power almost equaled the dynamic power. Hence, efficient leakage power reduction methods are very critical for the deep-submicron and nanometer circuits.

Although power consumption is important for modern VLSI design, operation speed and occupied area are still the main requirements of the VLSI design.

Multi threshold voltage CMOS (MTCMOS) technology is a good solution which provides a high performance and low-power design without any area overhead. Multi-threshold voltages are provided for each transistor in modern process technology. This paper describes low-power and high speed design for full adder, 4-bit ripple carry adder and 4×4 multiplier circuits with MTCMOS technology. This paper is organized as follows: Section II provides the circuit design with MTCMOS technology. Results are presented in Section III, followed by conclusions in Section IV.

II. CIRCUIT DESIGN WITH MTCMOS TECHNOLOGY

MTCMOS technology provides a solution to the high performance and low power design requirements of modern designs. MTCMOS technology provides the transistors that have low, normal and high threshold voltage [4]. This technology is an effective circuit level technique that provides a high performance and low-power design by utilizing both low and high threshold voltage transistors.

Low-threshold voltage transistors have high-speed performance but high-power consumption. High-threshold voltage transistors have low-power consumption but low-speed performance.

While the low-threshold voltage transistors are used to reduce the propagation delay time in the critical path, the high-threshold voltage transistors are used to reduce the power consumption in the shortest path [5], [6], [7]. This paper describes a low-power and high speed design for full adder, 4-bit ripple carry adder and 4×4 multiplier circuits with MTCMOS technology.

A. Design of full adder

When we add three bits A, B and C_{in} (input carry), then the Boolean function of the sum and carry are given as

following.

Sum = A ⊕ B

Carry = AB + (A ⊕ B) C_{in}

Fig. 2 shows the logic diagram of 1-bit full adder cell. The full adder contains 3 inputs (A, B, C_{in}) and 2 outputs (Sum and Carry). For the full adder circuit, carry path is the longest path and sum path is the shortest path.

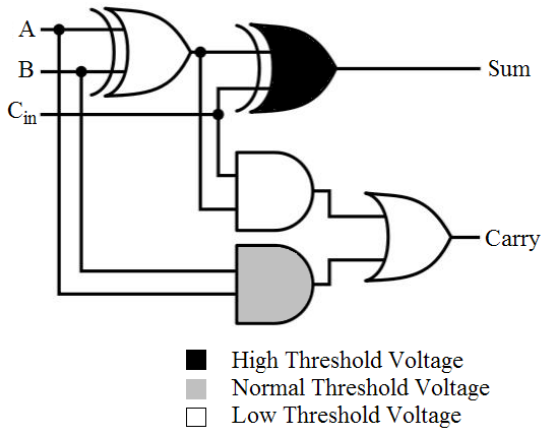


Fig. 2 Logic diagram for 1-bit full adder.

We use low-threshold voltage transistors, normal-threshold voltage transistors and high-threshold voltage transistors in the circuit design. Since carry path is the longest path in the circuit, the low-threshold voltage transistors are used in this path to reduce the propagation delay time in the critical path.

The second exclusive-OR gate present in the sum path is designed with high-threshold voltage transistors to reduce the power consumption in the shortest path. The remaining AND gate is designed with normal-threshold voltage transistor.

B. Design of 4-bit ripple carry adder

Fig. 3 shows the logic diagram of 4-bit ripple carry adder. The 4-bit ripple carry adder contains 9 inputs (A_0, A_1, A_2, A_3, B_0, B_1, B_2, B_3 and C_{in}) and 5 outputs (Sum_0, Sum_1, Sum_2, Sum_3 and Carry). For the ripple carry adder, Carry path is the longest path and the paths Sum_0, Sum_1, Sum_2 and Sum_3 are shorter when compared to the carry path.

We use low-threshold voltage transistors, normal-threshold voltage transistors and high-threshold voltage transistors in the circuit design. Since carry path is the longest path in the circuit, the low-threshold voltage transistors are used in this path to reduce the propagation delay time in the critical path.

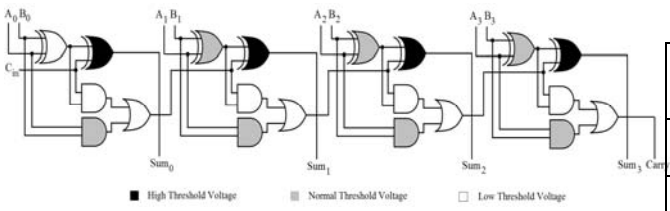


Fig. 3 Logic diagram of 4-bit ripple carry adder

The second exclusive-OR gates in each full adder cell are designed with high-threshold voltage transistors to reduce the power consumption in the shortest paths. The remaining gates are designed with normal-threshold voltage transistors.

C. Design of 4×4Multiplier

The logic diagram of 4×4 multiplier is shown in the fig. 4. The 4×4 multiplier circuit 8 inputs (a_0, a_1, a_2, a_3, b_0, b_1, b_2 and b_3) and 8 outputs (P_0, P_1, P_2, P_3, P_4, P_5, P_6 and P_7).

The output P7 is the critical path (longest path) in this circuit. This critical path contains 2 half adders and 4 full adders as shown in the figure. The carry paths in each of these 6 adders are designed with low-threshold voltage transistors to reduce the propagation delay time in the critical path.

The sum path in each of these 6 adders (the exclusive-OR gates in each of these 6 adders which gives the outputs P_1, P_2, P_3, P_4, P_5 and P_6) and the AND gate which gives the output P_0 are designed with high-threshold voltage transistors to reduce the power consumption in the shortest paths. The remaining gates are designed with normal-threshold voltage transistors.

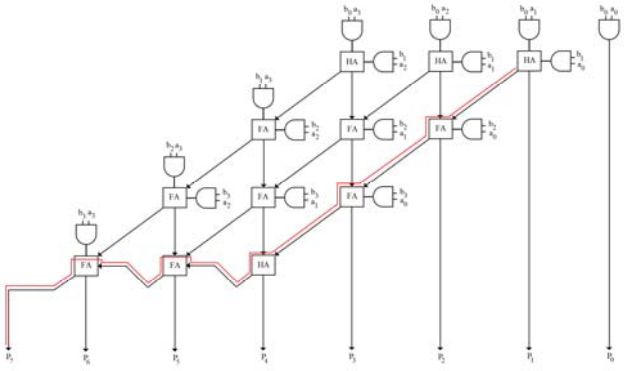


Fig. 4 Logic diagram of 4×4 Multiplier

III. RESULTS

The proposed full adder, ripple carry adder and multiplier circuits are simulated through HSPICE simulation using 45nm technology. The supply voltage for 45nm technology is 1.0V [1].

Table 1 shows the comparison table between the conventional full adder circuit and the proposed circuit. The comparison between the conventional 4-bit ripple carry adder and the proposed circuit is shown in the table 2 and table 3 shows the comparison table between the conventional 4×4 multiplier circuit and the proposed circuit.

TABLE I
COMPARISON TABLE FOR FULL ADDER CIRCUIT

	Conventional circuit	**MTCMOS**	**% reduction**
Static power (Watts)	2.311E-5	1.764E-5	23.66%
Delay in critical path(Sec)	2.599E-11	2.483E-11	4.46%

TABLE IIIII
COMPARISON TABLE FOR 4-BIT RIPPLE CARRY ADDER

	Conventional circuit	MTCMOS	% reduction
Static power (Watts)	9.308E-5	7.292E-5	21.65%
Delay in critical path(Sec)	6.814E-11	6.460E-11	5.19%

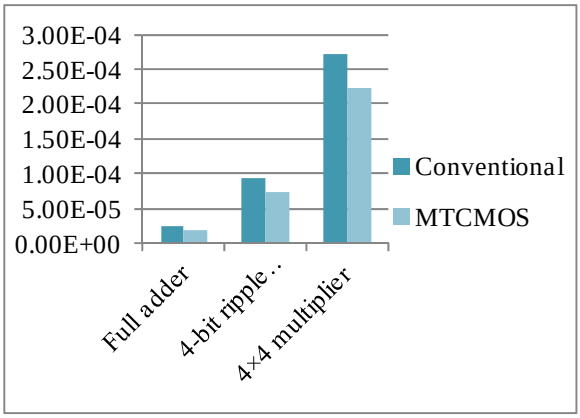
TABLE IVVVI
COMPARISON TABLE FOR 4×4 MULTIPLIER CIRCUIT

	Conventional circuit	MTCMOS	% reduction
Static power (Watts)	2.730E-4	2.238E-4	18.02%
Delay in critical path(Sec)	5.481E-11	5.317E-11	3.00%

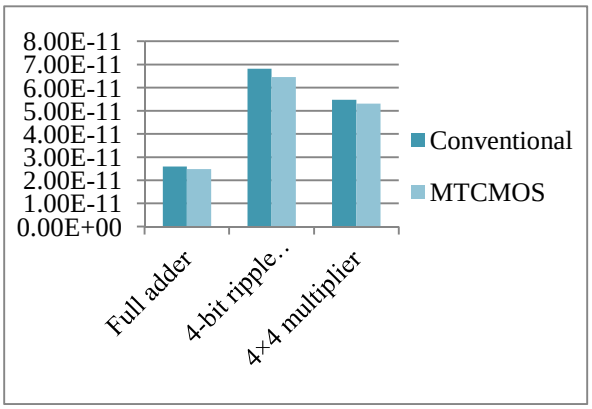
The proposed full adder circuit is achieved to reduce the power consumption by 23.66% and the propagation delay time by 4.46%.

The 4-bit ripple carry adder is achieved to reduce the power consumption by 21.65% and the propagation delay time by 5.19%.

The 4×4 multiplier is achieved to reduce the power consumption by 18.02% and the propagation delay time by 3.00%. Experimental results are shown in fig. 5.



a) Static power



b) Propagation delay

Fig. 5 Results for full adder, 4-bit ripple carry adder and 4×4 multiplier circuits for 45nm.

IV. CONCLUSIONS

In this paper, low-power and high speed CMOS logic circuits are designed using MTCMOS technology. The propagation delay time in the critical path is reduced by using low-threshold voltage transistors.

The power consumption is reduced in the shortest path by using high-threshold voltage transistors. Since there is no additional circuitry added in this technique, there will be no area overhead to the proposed circuits.

For 45nm technology, the proposed full adder circuit is achieved to reduce the power consumption by 23.66% and the propagation delay time by 4.46% compared to the conventional circuit. The 4-bit ripple carry adder is achieved to reduce the power consumption by 21.65% and the propagation delay time by 5.19% compared to the conventional circuit. The 4×4 multiplier circuit is achieved to reduce the power consumption by 18.02% and the propagation delay time by 3.00% compared to the conventional circuit.

REFERENCES

[1] International Technology Roadmap for Semiconductors (http://public.itrs.net/).

[2] B. J. Sheu, D. L. Scharfetter, P. K. Ko, and M. C. Jeng, "BSIM: Berkeleyshort-channel IGFET model for MOS transistors," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 558–566, Aug. 1987.

[3] S. Thompson, P. Packan, and M. Bohr, "MOS scaling: Transistor challenges for the 21st century," *Intel Technol. J.*, vol. Q3, 1998.

[4] Dong Whee Kim, Jeong Beom Kee, "Low-Power Carry Look-Ahead Adder With Multi-Threshold Voltage CMOS Technology", in Proceeding of *ICSICT* International Conference on *Solid-State and Integrated-Circuit Technology*, pp. 2160-2163, 2008.

[5] L.Wei, Z. Chen, M. Johnson, K. Roy, Y. Ye, and V. De, "Design and optimization of dual threshold circuits for low voltage low power applications," *IEEE Trans. VLSI Systems*, pp. 16–24, Mar. 1999.

[6] P. Pant, V. K. De, and A. Chatterjee, "Simultaneous power supply, threshold voltage, and transistor size optimization for low-power operation of CMOS circuits," *IEEE Trans. VLSI Syst.*, vol. 6, pp. 538–545, Dec. 1998.

[7] Q. Wang and S. Vrudhula, "Static power optimization of deep sub-micron CMOS circuits for dual V_t technology," in *Proc. ICCAD*, Apr. 1998, pp. 490–496.